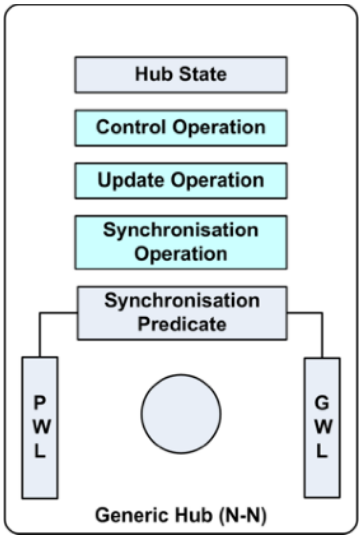
VirtuosoNext™

A scalable and Network Centric RTOS for Embedded Applications, enabling safe and secure small grain Space and Time Partitioning

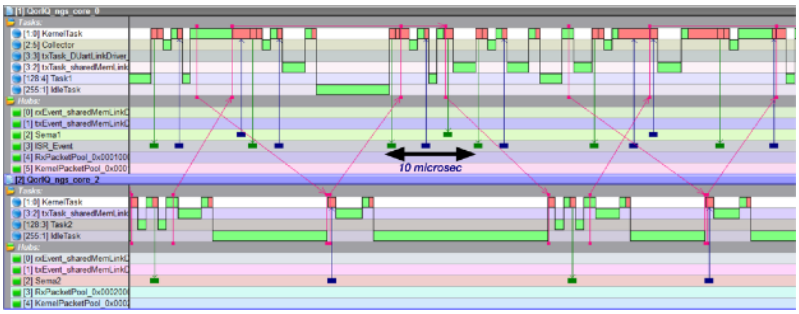


VirtuosoNext™ breaks new grounds in the field of Real-Time Operating Systems. It was from the ground up developed using **formal modeling,** enabling **safety critical and high reliability** applications, Conceptually it was developed as a scalable communication layer to support **heterogeneous multi-processor** systems, but it runs equally well on a single processor. It supports small microcontrollers, **many-core** chips with little memory as well as **widely distributed systems**.
The **Virtual Single Processor** programming model provides transparent parallel processing. An additional benefit of the unique architectural approach is safety and scalability. VirtuosoNext™ provides the same kernel services as most RTOS, such as starting and stopping tasks, **priority based preemptive scheduling supporting priority inheritance, Events, Semaphores, FIFOs, Ports, Hubs, Resources, Memory Pools but also BlackBoards, DataEvents and MemoryBlockQueues**. With VirtuosoNext, the user can also enable **fine-grain space and time partitioning**. This provides hypervisor like protection but keeps the reactivity of a fast RTOS. Each application task is fully protected in memory. Upon a fault, the CPU exception is trapped and the task is restored in microseconds enabling real-time fault tolerance.

Entirely written in ANSI-C (MISRA checked) the full code size will vary between about 5 to 30 Kbytes, whereas the code generation tools will remove any unused functionality. Services can be called in blocking, non-blocking, blocking with time-out and asynchronous mode. The kernel itself as well as the drivers are also tasks, increasing the modularity and reducing the critical sections.

From the RTOS point of view the kernel shuffles Packets around, while for the implementation the Hubs play the dominant role. Packets are sent to a Hub where they synchronise with requests from other tasks. If no request is available, the Packets are put in a priority ordered waiting queue. By design, such buffers cannot overflow. VirtuosoNext™ has also unique support for distributed priority inheritance.

Simulation is very important, therefore Microsoft Windows and Linux are supported as virtual hardware nodes. While this simulator provides for logically correct operations, it also allows integrating existing host operating systems or existing RTOS with the nodes running VirtuosoNext. A simple serial connection can be sufficient to establish communication. The Event Tracer allows the user to analyse task scheduling and inter-node interaction.



VirtuosoNext has also integration support via the version management repository with the GoedelWorks™ project development environment for traceability. A **Qualification package** is also available as a project developed inside Altreonic's GoedelWorks.

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Available services	
Hub Enity	**Semantics**
Event	Synchronisation on a boolean event
DataEvent	Event Synchronisation with data transfer
Counting Semaphore	Synchronisation on a positive counter
FIFO queue	Buffered communication
Resource	Creates a logical critical section
Port	Exchanging Packets
Packet pool	Dynamic Packet allocation
Memory Block pool	Dynamic memory allocation
MemoryBlock Queue	Locally buffered communication (SP only)
Single phase services	
_W	Tasks waits for synchronisation
_WT	Tasks waits until synchronisation or timeout
_NW	Task returns immediately
Two phase services	
_Async	Task returns and synchronises later (SP only)
Tools	
Visual Designer	A graphical Modeling and application development environment with target metamodels and code generator
Event Tracer	A visual and analysing display of intra- and internode events
Open System Inspector	For easy use of a host-node and its service
Host server component	For easy use of host nodes and their services
Board/Processor Support Package	On request
Safe Virtual Machine	Target independent execution of binary code

Performance metrics (-Os compiled)				
Protection	**Disabled**		**Enabled**	
CPU	ARM-M3	PPC-e600	ARM-M3	ARM-A9
Code Size*				
Minimum	4496	9116	8024	15004
Max. (all services)	8656	15724	11564	21844
Performance: semaphore loop (in clock cycles) = 4 services + 4 context switches)				
	2745	3826	2945	10423
Interrupt latency (in clock cycles) Measured as time interval between the HW interrupt and reading data				
IRQ to ISR	46	550**	50	197***
IRQ to Task	754	1990**	850	2465***

*Measured by building a minimum application, including the compiler added runtime libraries (which is processor specific). No MBQ for disabled mode.
**: measured at board level (Curtis Wright VME-183 Dual Freescale 7447A/7448 SBC). Includes external interrupt controller.
***: OMAP 4460

While already rich in semantic behaviour, more elaborate and specialised services can be added using the **generic Hub**, an implementation of Guarded Actions complemented by **callback functions.**
VirtuosoNext transparently supports heterogeneous target systems allowing to mix 8bit, 16bit, 32bit, 64bit and DSP processors, FPGA co-processing blocks or even host nodes running a traditional (RT)OS. The only requirement is the availability of an ANSI-C compiler. A POSIX conversion kit is available as well. The code is statically linked with datastructures being generated at build time reducing memory requirements as well as increasing safety The developer specifies his topology and application using Visual Designer™ or by editing the configuration files. Fine grain space and time partitioning is enabled depending on the target node.For the first time trustworthiness is combined with small code size, performance and ease of use, also for heterogeneous distributed applications.
VirtuosoNext is a concurrent programming paradigm that was designed to be used. VirtuosoNext is not just another RTOS. It reinvents the very concept. Available under an Open Technology Licensing scheme. Qualification Package available as a GoedelWorks project.

Altreonic